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**Patentanmeldung Nr. | Patent application No. | Demande de brevet n°**

02368141.4

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

**R C van Dijk**

Anmeldung Nr:
Application no.: 02368141.4
Demande no:

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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If no title is shown please refer to the description.
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An improved differential sampling circuit for generating the differential input signal DC offset

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
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H03M1/00

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL
PT SE SI SK TR

# AN IMPROVED DIFFERENTIAL SAMPLING CIRCUIT FOR GENERATING THE DIFFERENTIAL INPUT SIGNAL DC OFFSET

## FIELD OF THE INVENTION

The present invention relates to analog circuits and more particularly to an improved differential sampling circuit based on a switched-capacitor approach that directly generates the real differential signal DC offset value.

## BACKGROUND OF THE INVENTION

With the continuous frequency increase of signals used in modern communication links, unwanted effects such as cross talk, false ringing, parasitic reflection, offset.... occur more and more often due to the distributed nature of the media which transports these signals. In the particular case of coupled lines, a major contributor is the differential input DC offset which is the result of different amplitudes and common modes on each of the lines. For instance, according to the SCSI standard for hard-disk applications (SPI4) effective to date, data are transported at 80 MHz (frequency of the system clock). At this speed, the data integrity on the bus is high enough and substantially do not require any offset cancellation technique. On the contrary, according to the next SCSI standard to be implemented in the future (SPI5) data will be transported at 160 MHz. At such a very high speed, the compensation of the differential input signal DC offset becomes absolutely mandatory. This differential input signal

DC offset must be sampled and stored in a capacitor. Then, an analog to digital converter (ADC) converts this value in binary digits and stores it in a register latch.

FIG. 1 illustrates the definition of the differential input signal DC offset. As apparent in FIG. 1, the amplitudes and common modes of a differential signal VP-VN are different between the first half and the second half of the period T of the system clock. The differential input signal DC offset is defined as being equal to the half sum of the differential amplitude $\Delta V1$ in the first half period and the differential amplitude $\Delta V2$ in the second half period. The differential input signal DC offset $\Delta Voffset$ is given by relations: $0.5*[(VP1+VP2)-(VN2+VN1)]$ or $0.5*[(VP1-VN1)+(VP2-VN2)]$, i.e. Finally $0.5*[\Delta V1+\Delta V2]$. This calculation can be performed by a sampling circuit which samples the differential input signal twice within a clock cycle and has a gain of 1/2.

The conventional differential input signal sampling circuit disclosed in the following reference: "A ratio-Independent Algorithmic Analog-to-digital conversion technique", IEEE JSSC, vol 19, pp 828-836, December 1984, by P.W. Li, M.J. Chin, P.R. Gray, and R. Castello is of interest in some respects. It is constructed around a differential operational amplifier (opamp) provided with a switched-capacitor network in order to sample twice the differential input signal in four phases to generate $2*\Delta V$, if the input signal keeps its value at times of sampling or $[\Delta V1+\Delta V2]$, if not. Although, it does not aim to calculate the differential input signal DC offset, its gain is independent of both the opamp DC offset and the capacitor values which is a determining advantage.

FIG. 2 shows the single-ended version (simplified diagram) of this conventional differential input signal sampling circuit referenced 20, which samples twice the input signal Vin, to

generate a signal Vout = Vin+Vin = 2*Vin, if input signal Vin remains unchanged during the sampling operations. The single ended version has been chosen in lieu of the differential one for the sake of simplicity of the description. Now turning to FIG. 2, circuit 20 is organized around an operational amplifier (opamp) 21 and a switched-capacitor network comprising two capacitors C1, C2 and six switches S1-S6 connected as shown in FIG. 2. The positive input of the opamp 21 is coupled to the ground. A first capacitor C1, usually referred to as the holding capacitor, is coupled to its negative input and a first node 22. A first switch S1 is coupled between said first node 22 and the input signal Vin. A second switch S2 is coupled to said first node 22 and the ground. A second capacitor C2 is coupled between a second node 23 and the opamp 21 negative input. A third switch S3 is coupled between said negative input and the output of opamp 21. A fourth switch S4 is coupled to said second node 23 and said output. A fifth switch S5 is coupled between said second node 23 and the ground. Finally, a sixth switch S6 is coupled to said first node 22 and said output in a feedback loop. Output signal Vout that is generated by circuit 20 is independent of the opamp 21 DC offset Voff and of the value of capacitors C1 and C2. Operation of circuit 20 will be described by reference to FIGS. 2a-2d. From one drawing to the next one, the status of switches S1-S6 changes. They can be opened or closed according to the application algorithm.

Circuit 20 full operation requires four phases : two input signal sampling and two charge transfers. Considering FIG. 3a, let us assume the input signal to be sampled Vin is equal to V1. It is easy to calculate voltage Vc1 across capacitor C1, voltage Vc2 across capacitor C2 and output voltage Vout. At the end of the first input signal sampling, we have:

$$Vc1 = V1-Voff$$

$$Vc2 = -Voff$$

Vout = Voff

The charge Q1 stored into capacitor C1 is equal to C1.(V1-Voff)

After the first sampling, the first charge transfer is performed using the configuration shown in FIG. 3b. The charge variation DQ1= C1*V1 is transferred in capacitor C2. We then have:

Vc1 = -Voff
Vc2 = -Voff+V1*C1/C2
Vout = V1*C1/C2

The first sampling and the first charge transfer described above by reference to FIGS. 3a-3b are performed during the first half period of the system clock.

Next, the second input signal sampling is performed using the configuration depicted in FIG. 3c. After the second input sampling, we assume that Vin has changed and is now equals to V2. We have:

Vc1 = V2-Voff
Vc2 = -Voff+V1*C1/C2 (Vc2 remains unchanged)
Vout = Voff

Finally, the second charge transfer is performed using the configuration shown in FIG. 3d. At the end of this step, the charge Q2 stored on C2 is transferred in capacitor C1 so that we have:

Vc2 = -Voff
DQ2 = V1*C1
Vc1 = V2-Voff+DQ2/C1 = V2-Voff+V*C1/C1 = V1+V2-Voff
Vout = Voff+Vc1 = V1+V2

The second sampling and the second charge transfer described above by reference to FIGS. 3c-3d are performed during the second half period of the system clock. The operations described above by reference to FIGS. 3a-d are thus performed at each system clock cycle.

Consequently, using circuit 20, Vout equals the sum of the two sampled input values V1 and V2. It is to be noted that Vout is independent of both the opamp 21 DC offset Voff and the values of capacitors C1 and C2 which is beneficial. However, should we consider the differential version of circuit 20 applied to the calculation of the differential DC offset $\Delta$Voffset, it would generate a differential voltage equal to [$\Delta$V1+$\Delta$V2], so that it would have the inconvenience of requiring a 1/2 gain opamp connected in series at its outputs before obtaining the differential offset value which is equal to 0.5*[$\Delta$V1+$\Delta$V2].

## SUMMARY OF THE INVENTION

According to the present invention there is described an improved differential sampling circuit based on a switched-capacitor network approach that directly generates the real differential input signal DC offset value. It is configured around a differential operational amplifier and is provided with a pair of switched-capacitor networks, each including an innovative block to generate the real value of the differential input signal DC offset at each system clock cycle. During the first half cycle, the differential input signal pair is sampled and the holding capacitors in each network are charged. During the second half cycle, the differential input signal pair is sampled again and the holding capacitors are further charged. At the end of the cycle, the charges held in the holding capacitors are applied to the differential operational amplifier, so that the

differential output signal that is output therefrom is equal to the real differential input signal DC offset value.

It is therefore a primary object of the present invention to provide an improved differential sampling circuit based on a switched-capacitor network approach that directly generates the real differential input signal DC offset value.

It is another object of the present invention to provide an improved differential sampling circuit configured around a differential operational amplifier and a pair of switched-capacitor network wherein the differential input signal DC offset value is independent of the differential operational amplifier DC offset.

It is still another object of the present invention to provide an improved differential sampling circuit based on a switched-capacitor network approach that directly generates the differential input signal DC offset value with a high accuracy to meet the SCSI-PI5 specifications.

The novel features believed to be characteristic of this invention are set forth in the appended claims. The invention itself, however, as well as other objects and advantages thereof, may be best understood by reference to the following detailed description of an illustrated preferred embodiment to be read in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates the general definition of the differential input signal DC offset.

FIG. 2 is a schematic diagram of a conventional single-ended input signal sampling circuit.

FIGS. 3a-d shows different configurations of the FIG. 2 circuit to illustrate its four operational phases.

FIG. 4 shows the single-ended input signal sampling circuit of FIG. 1 improved according to the present invention.

FIGS. 5a-d shows different configurations of the FIG. 4 circuit to illustrate its four operational phases.

FIG. 6 is a schematic diagram of the improved differential sampling circuit for generating the real differential input signal DC offset value of the present invention which derives from the FIG. 4 circuit.

## DESCRIPTION OF A PREFERRED EMBODIMENT

Like reference numerals (with prime) are used through the several drawings to designate identical (corresponding) parts. For the sake of illustration, the circuit 20 shown in FIG. 2, will be first modified to generate 0.5*(V1+V2) instead of (V1+V2) according to the present invention.

As apparent in FIG. 4, where the improved circuit is referenced 40, the modification consists to add innovative circuit block 41 which comprises one extra capacitor C0 and two extra switches S7 and S8. Capacitor C0 is coupled to the opamp 21 negative input and to a third node 42. Switch S7 is coupled to said second node 42 and the ground. Switch S8 is connected between said first and third nodes.

The operation of improved circuit 40 is still based upon four operational phases that will be now described by reference to FIGS 5a-5d, that are performed at each system clock cycle.

Let us consider FIG. 5a which illustrates the first input signal sampling. Let us still assume Vin = V1. When V1 is sampled, the capacitor C0 is floating as switches S7 and S8 are open. Switches S2, S4 and S6 are open while switches S1, S3 and S5 are closed. After the first input signal sampling, we have:

Vc1 = V1-Voff
Vc2 = -Voff
Vout = Voff

The charge Q1 stored into holding capacitor C1 is equal to C1*(V1-Voff).

FIG. 5b illustrates the configuration of improved circuit 40 during the first charge transfer when switches S1, S3 and S5 are opened and switches S2 and S4 are closed. During this phase, the charge variation DQ1, equal to C1*V1, is transferred into capacitor C2, and we have:

Vc1 = -Voff
Vc2 = -Voff + V1*C1/C2
Vout = V1*C1/C2

During the second input sampling, switches S1, S3 and S7 are closed and switches S2 and S4 are opened, improved circuit 40 then has the configuration depicted in FIG. 5c. Let us assume now that Vin has changed and equals V2. The capacitor C0 is connected to ground because switch S7 is closed, so that we have:

Vc0 = - Voff
Vc1 = V2-Voff
Q1 = C1*(V2-Voff)
Vc2 = - Voff+V1*C1/C2 (Vc2 remains unchanged)
Vout = Voff

The charge Q0 stored into capacitor C0 is equal to -C0*Voff. This is an important feature of the present invention as it will appear more apparent in the following paragraph. The charge stored in capacitor C2 is equal to V1*C1-C2.Voff.

Finally, during the second charge transfer (see FIG. 5d), switches S1, S3 and S7 are opened while switches S5, S6 and S8 are closed. The capacitor C0 is put in parallel on capacitor C1 because switch S8 is closed. We then have:

$Vc2 = -Voff$

$Q2 = - Voff*C2$

$Vc0 = Vc1 = (Q0+Q1)/(C0+C1) = (C1*V2-Voff(C0+C1))/(C0+C1) = V2* C1/(C0+C1)-Voff$

There is a charge transfer equal to the charge variation DQ2 to capacitors C0 and C1. Consequently, the voltages Vc0 and Vc1 change as follows:

$DQ2 = C1*V1$

$Vc0 = Vc1 = (DQ2+Q0+Q1)/(C0+C1) = C1*V1/(C0+C1)+V2*C1/(C0+C1)-Voff$

$Vc0 = Vc1 =(V1+V2)/(1+C0/C1)-Voff$, and finally

$Vout = Vc0+Voff = (V1+V2)/(1+C0/C1)$.

Because $Q0=-C0*Voff$ is present in the calculation of Vc0, the opamp 21 DC offset Voff does not appear in Vout. As a result, the signal that is output from circuit 40 is still independent of the opamp 21 offset and the value of capacitor C2 as well. One may notice that, if C0 = C1, i.e. if there is a perfect matching between these capacitors, then $Vout = 0.5*(V1+V2)$, if not the error on Vout is divided by two. For instance, if the mismatch between C0 and C1 is equal to about 2%, the error on Vout will be about 1% only. Only the ratio C0/C1 of capacitor values must be as close as possible of 1. The improved differential sampling circuit for generating the real differential input signal DC offset of the present invention which will be now described in detail, comes straight from this circuit 40.

Now turning to FIG. 6, the improved differential sampling circuit which bears numeral 60 results of the combination of two identical circuits 40 driven by first and second input signals Vin+ and Vin- respectively. However, in the preferred implementation of the present invention shown in FIG. 6, the two opamps have been merged in a single differential opamp referenced 61, having thus two inputs and two outputs, for greater optimization. As apparent in FIG. 6, the upper switched-capacitor network 62′, which includes innovative block 41′, is connected between the positive input and the negative output. Likewise, the lower switched-capacitor network 62″, which includes innovative block 41″, is connected between the negative input and the positive output. In the upper network, the extra devices are referenced C0′, S7′ and S8′. In the lower network, the extra devices are referenced C0″, S7″ and S8″. Obviously, it is highly desirable that the corresponding components in the upper and lower networks are matched. The input signals applied to improved circuit 60, forming the differential input signal pair, are labeled Vin+ and Vin-. Corresponding output signals are labeled Vout- and Vout+ respectively, defining a differential output signal Δ Vout therebetween. By construction, this differential output signal ΔVout that is generated by improved circuit 60 is equal to the differential input signal DC offset ΔVoffset, as soon as the four operational phases have been completed. Vout- = 0.5*[(Vin+1)+(Vin+2)], Vout+ = 0.5*[(Vin-1)+(Vin-2)] using the calculations and the notations given above for the improved circuit 40 described by reference to FIGS. 4 and 5a-d, so that ΔVout = (Vout-) - (Vout+) = ΔVoffset = 0.5*[ΔV1+ΔV2], wherein ΔV1 = [(Vin+1)-(Vin-1)] and +ΔV2 = [(Vin+2)+(Vin-2)], i.e. to the half sum of the two sampled differential input signal values.

Simulations have demonstrated that it is possible to measure the real value of the differential input signal DC offset and then to meet the SCSI-PI5 specifications.

The advantages of the invention are recited below. The differential input signal DC offset value is measured during only one system clock period. The DC offset is independent of the differential opamp 61 DC offset and the values of capacitors. Only the capacitor value ratio C0/C1 must be equal to 1, a mismatch in this ratio of x% would lead to an error of x/2% in the measured DC offset value.

While the invention has been particularly described with respect to a preferred embodiment thereof it should be understood by one skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

# CLAIMS

What is claimed is:

1. An improved differential sampling circuit (60) based on a switched-capacitor approach that generates the real differential input signal DC offset value at each period of a system clock comprising:

first and second input signals (Vin+,Vin-);

clock generating means to generate a system clock;

a differential operational amplifier (61) having a positive input, a negative input, a positive output that generates a first output signal Vout+ and a negative output that generates a second output signal Vout- defining a differential output signal ΔVout therebetween;

in a first switched-capacitor network (62'):

a first capacitor (C1') coupled to said positive input and a first node (22');

a first switch (S1') coupled to said first node and a first input signal (Vin+);

a second switch (S2') coupled to said first node and the ground; a third switch (S3') coupled to said positive input and said negative output;

a fourth switch (S4') coupled to said negative output and a second node (23');

a fifth switch (S5') coupled to said second node and the ground;

a second capacitor (C2') coupled to said positive input and second node;

a sixth switch (S6') coupled to said first node and negative output;

a third capacitor (C0') coupled to said positive input and a third node (42');

a seventh switch (S7′) coupled to said third node and the ground; a eight switch (S8′) coupled to said first and third nodes;

in a second switched-capacitor network (62″):

a fourth capacitor (C1″) coupled to said negative input and a fourth node (22″);

an ninth switch (S1″) coupled to said fourth node and second input signal (Vin-);

a tenth switch (S2″) coupled to said fourth node and the ground; an eleventh switch (S3″) coupled to said negative input and said positive output;

a twelfth switch (S4″) coupled to said positive output and a fifth node (23″);

a thirteenth switch (S5″) coupled to said fifth node and the ground;

a fifth capacitor (C2″) coupled to said negative input and fifth nodes;

a fourteenth switch (S6″) coupled to said fourth node and positive output;

a sixth capacitor (C0″) coupled to said third negative input and a sixth node (42″);

a fifteenth switch (S7″) coupled to said sixth node and the ground;

a sixteenth switch (S8″) coupled to said fourth and sixth nodes; wherein said first and third capacitors have equal values;

wherein said fourth and sixth capacitors have equal values; and,

wherein said first to sixteenth switches are responsive to control signals to be selectively set in either the "open" or "close" state according to a determined algorithm within one period of said system clock.

2. The improved sampling circuit of claim 1 wherein said control signals are generated by timing control means receiving the system clock.

3. The improved sampling circuit of claim 1 wherein the first/ninth, third/eleventh and fifth/thirteen switches are closed while the second/tenth, fourth/twelfth, sixth/fourteenth, seventh/fifteenth and eighth/sixteenth switches are open during at least a first portion of the first half period.

4. The improved sampling circuit of claim 1 wherein the second/tenth, fourth/twelfth switches are closed while the first/ninth, third/eleventh, fifth/thirteen, sixth/fourteenth, seventh/fifteenth and eighth/sixteenth switches are open during at least a second portion of the first half period.

5. The improved sampling circuit of claim 1 wherein the first/ninth, third/eleventh and seventh/fifteenth switches are closed while the second/tenth, fourth/twelfth, fifth/thirteen, sixth/fourteenth and eighth/sixteenth switches are open during at least a first portion of the second half period.

6. The improved sampling circuit of claim 1 wherein the fifth/thirteen, sixth/fourteenth and eighth/sixteenth switches are closed while the first/ninth, second/tenth, third/eleventh, fourth/twelfth and seventh/fifteenth switches are open during at least a second portion of the second half period.

ABSTRACT

**AN IMPROVED DIFFERENTIAL SAMPLING CIRCUIT FOR GENERATING THE DIFFERENTIAL INPUT SIGNAL DC OFFSET**

The improved differential sampling circuit (60) of the present invention is configured around a differential operational amplifier (61) and is provided with a pair of switched-capacitor networks (62′,62″), each including an innovative block (41′,41″), to generate the real value of the differential input signal DC offset at each system clock cycle. During the first half cycle, the differential input signal pair (Vin+,Vin-) is sampled and the holding capacitors (C1′,C1″) in each network are charged. During the second half cycle, the differential input signal pair is sampled again and the holding capacitors are further charged. At the end of the cycle, the charges held in the holding capacitors are applied to the differential operational amplifier, so that the differential output signal ΔVout that is output therefrom is equal to the real differential input signal DC offset value.

FIG. 6

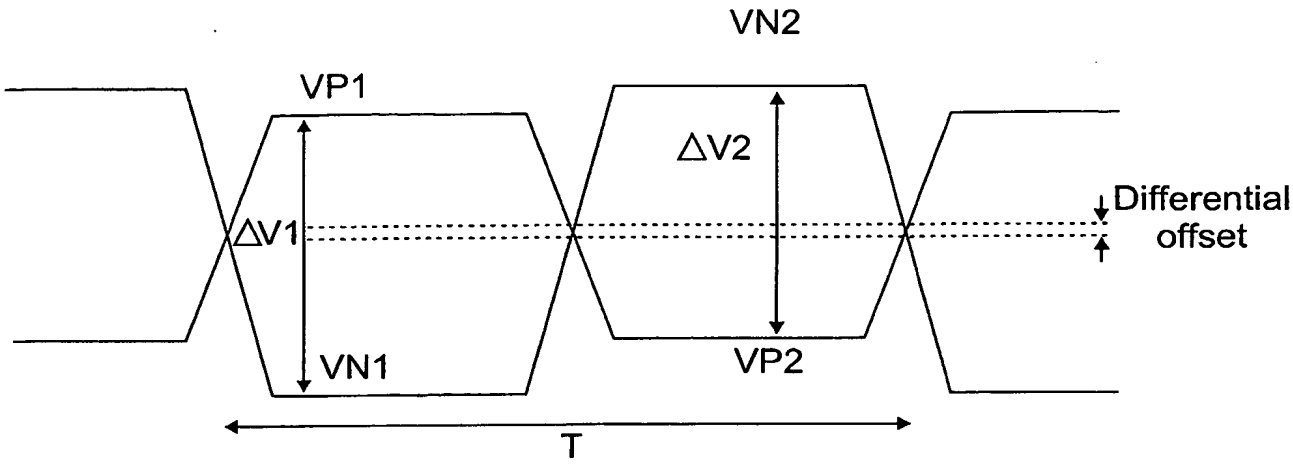


FIG. 1

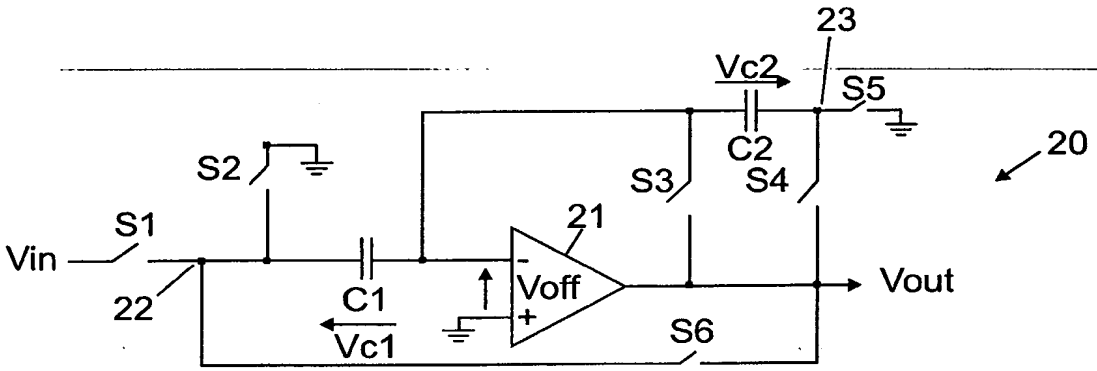


FIG. 2 (PRIOR ART)

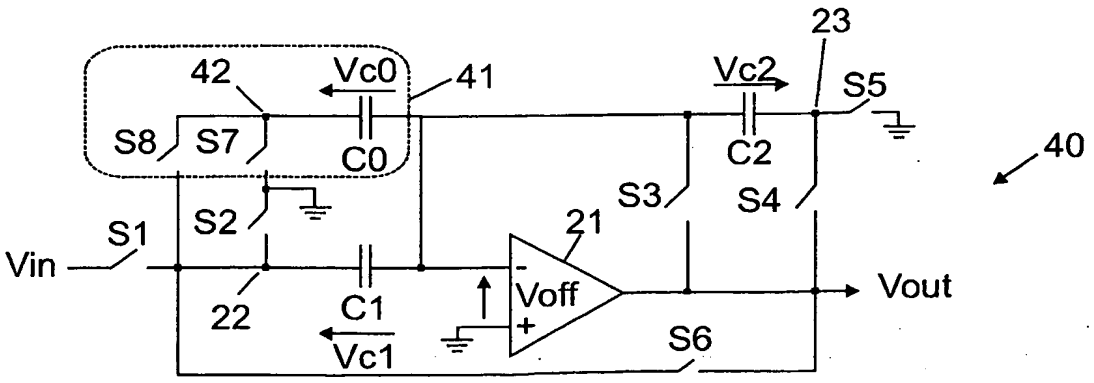


FIG. 4

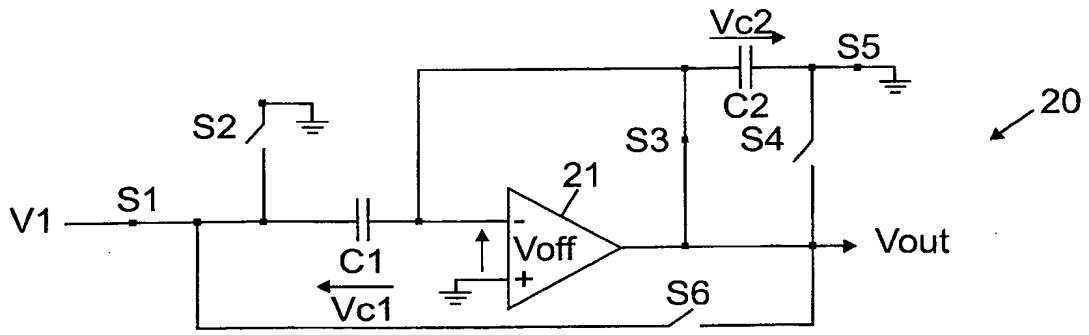


FIG. 3a (PRIOR ART)

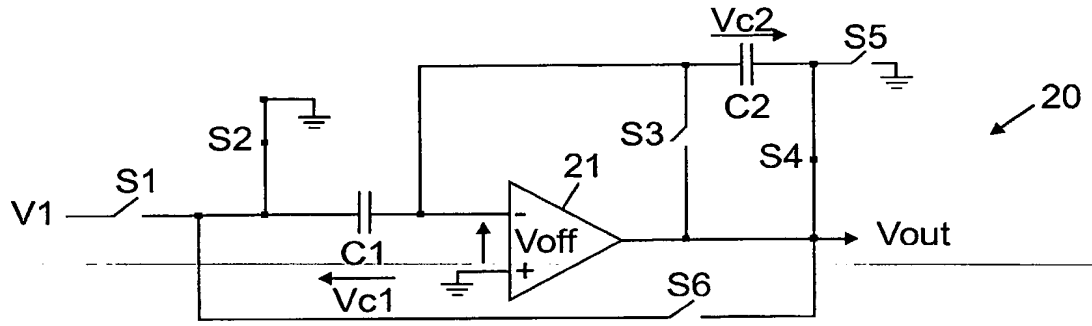


FIG. 3b (PRIOR ART)

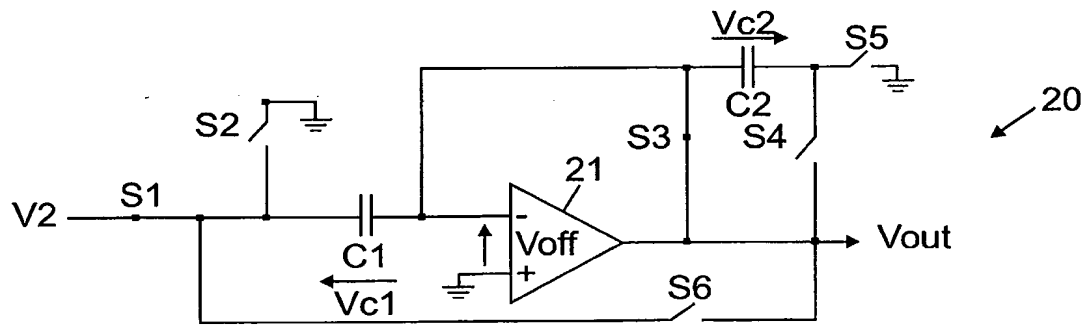


FIG. 3c (PRIOR ART)

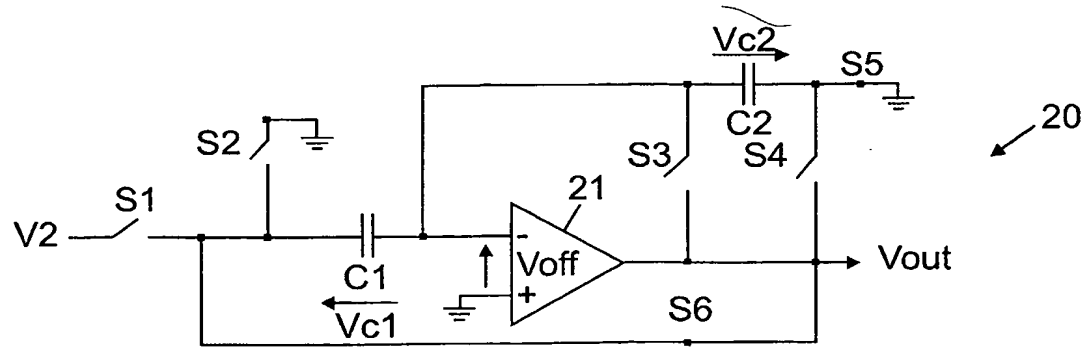


FIG. 3d (PRIOR ART)

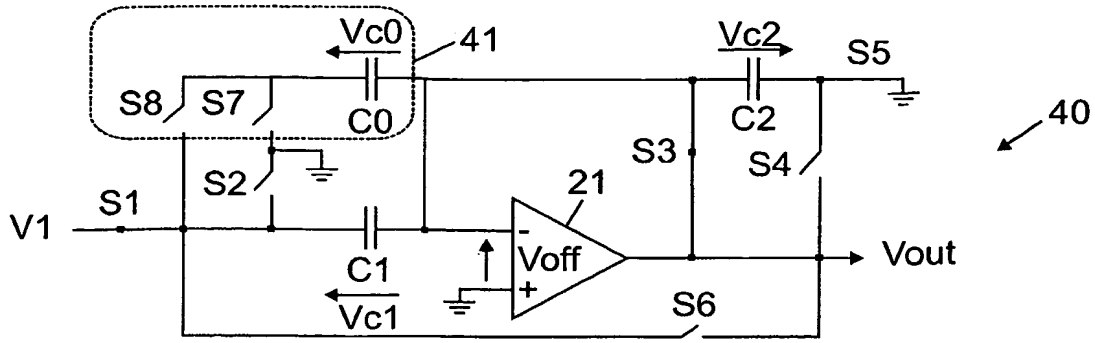


FIG. 5a

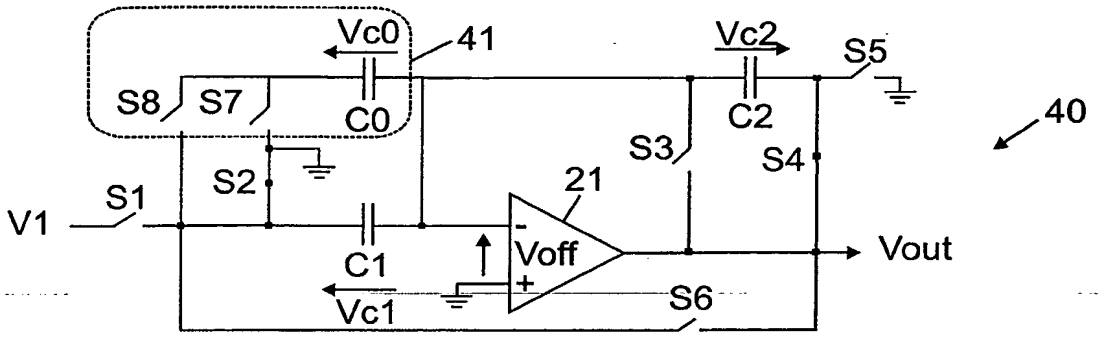


FIG. 5b

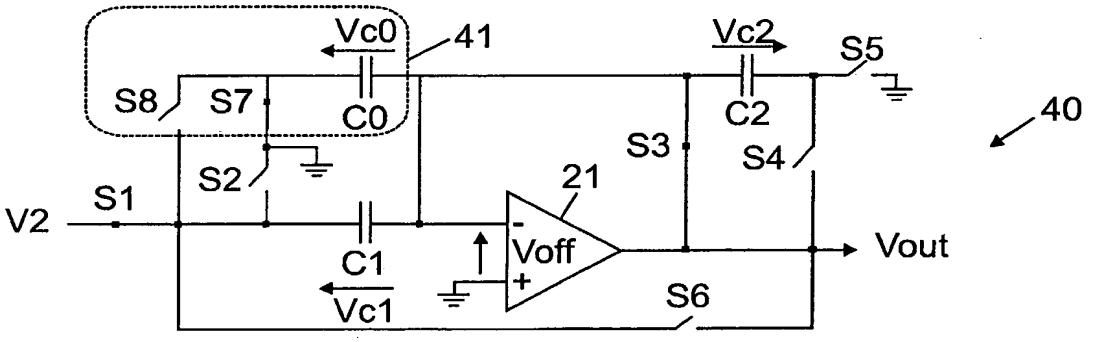


FIG. 5c

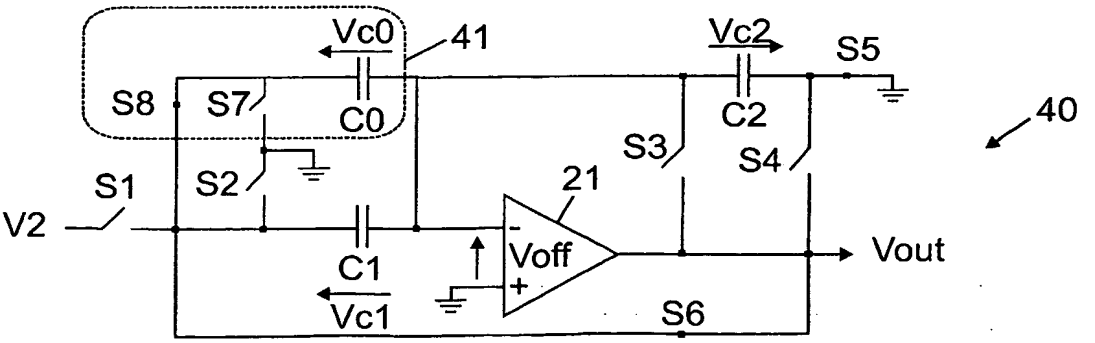


FIG. 5d

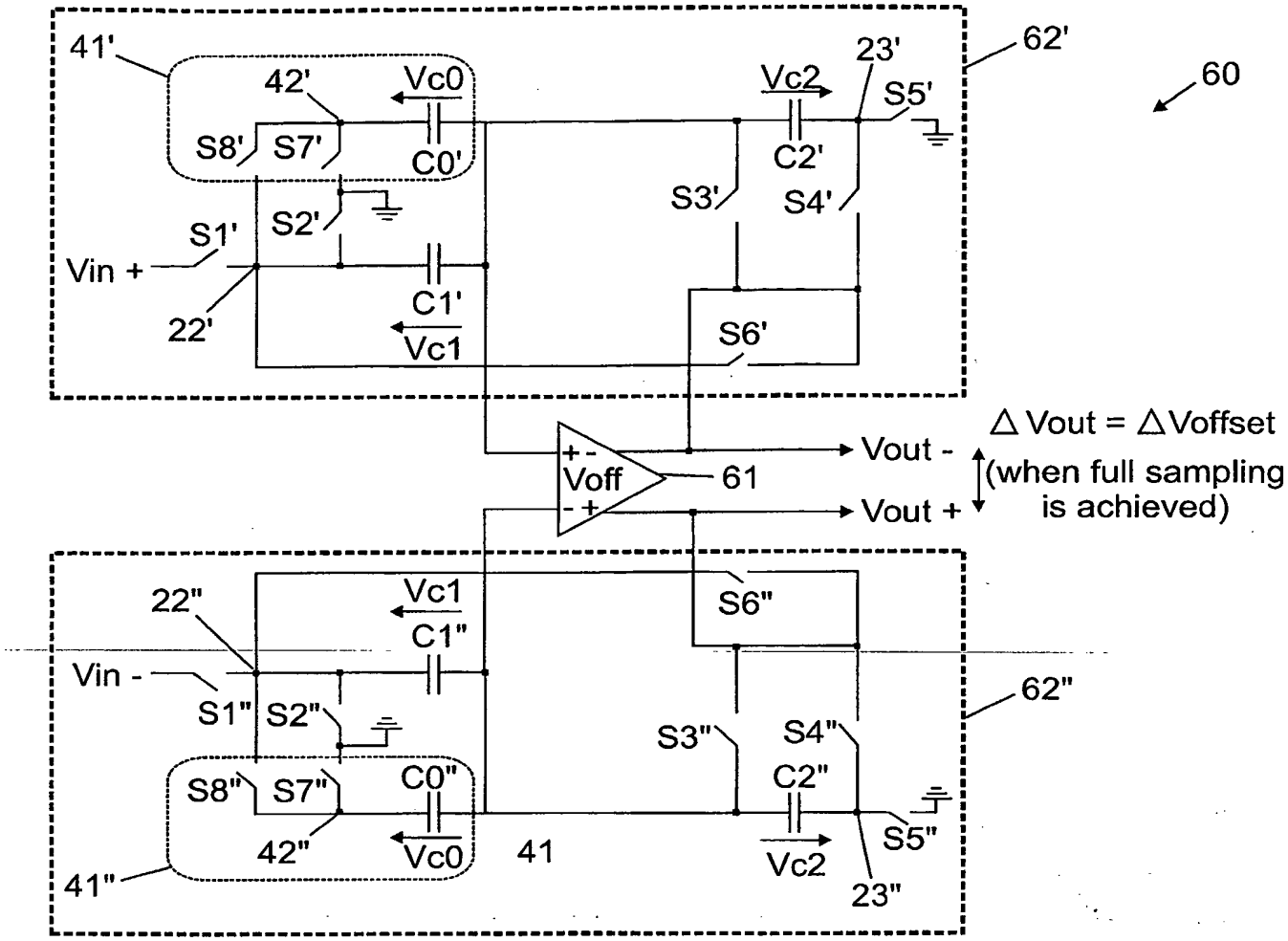
41'
42'
Vc0
S8'
S7'
C0'
S1'
S2'
Vin +
22'
C1'
Vc1
23'
Vc2
S5'
C2'
S3'
S4'
S6'
62'
60
+ -
Voff
- +
61
Vout -
Vout +
Δ Vout = Δ Voffset
(when full sampling
is achieved)
22"
Vc1
C1"
S6"
Vin -
S1"
S2"
S3"
S4"
62"
S8"
S7"
C0"
C2"
S5"
42"
Vc0
41
Vc2
23"
41"

FIG. 6